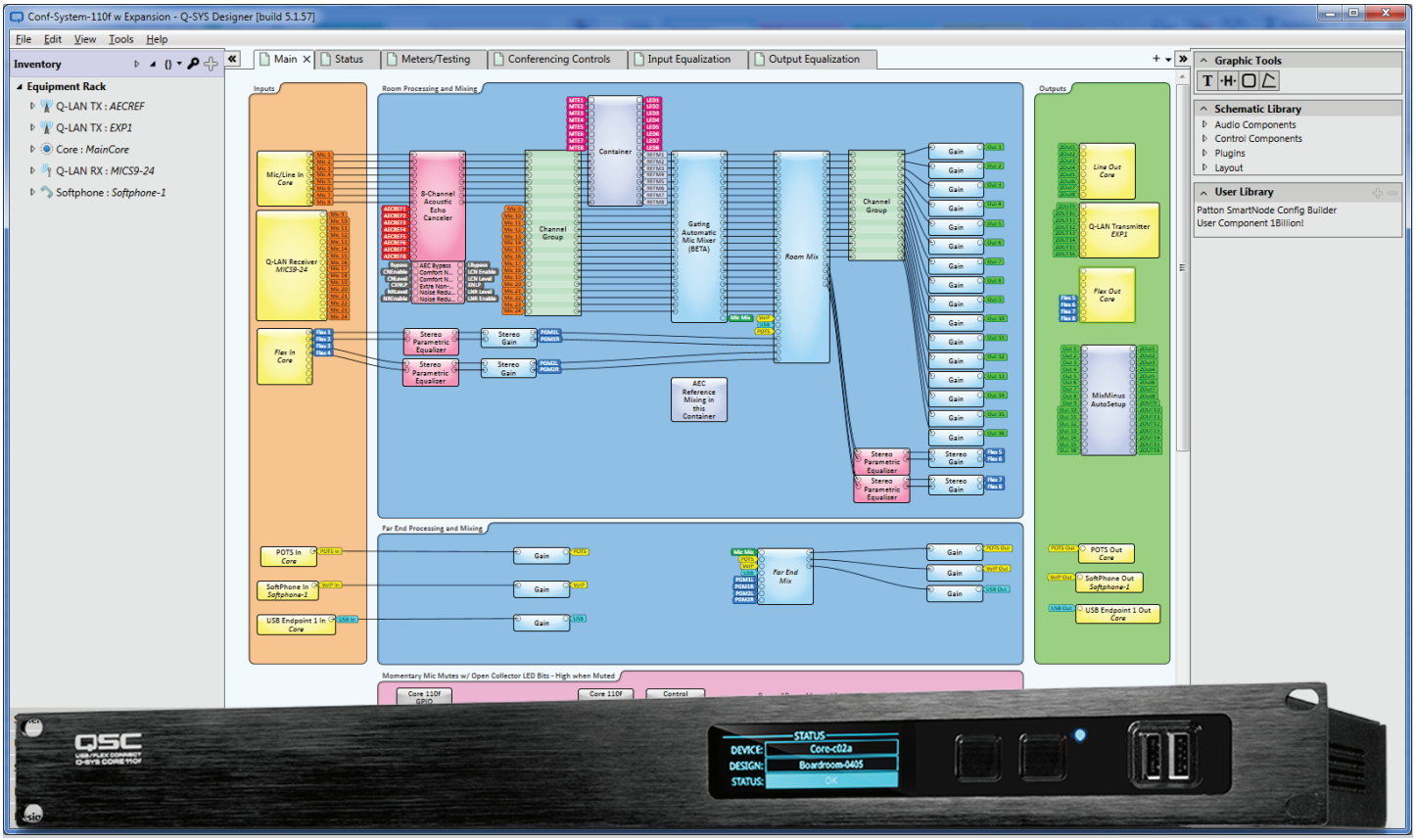
Application Guide

Q-SYS Core 110f Multiple core processors in a large conferencing system



Application Engineering Team

Rev. A, 22 July 2016

YES, YOU CAN CREATE A LARGE Q-SYS CONFERENCING NETWORK WITH MORE THAN ONE CORE 110F.

The Q-SYS Core 110f processor is a powerful tool for creating a great conferencing environment, but what if the need for AEC processing *exceeds* 16 channels? One could substitute a larger integrated or enterprise Q-Sys core processor, but it is possible to use a second Core 110f as an AEC expansion unit.

Q-SYS systems that consist of multiple core processors must be configured using a separate design file for each one, using Q-SYS Designer software. The core processors can share audio and control using Q-LAN audio streams and control link blocks. Then, once these links are configured and established, the cores can all operate as a single system. To help with getting started, there are example configuration files that can be modified as required to configure a multi-core processor system. There is a file for each of the 'main' and 'expansion' core processors. The appropriate Q-LAN streaming and Core-to-Core control links are already configured and ready to go. These default files support the following features:

- As many as 24 conferencing microphones
- GPIO mute switches and LED indicator signals
- 2 stereo codec/program sources
- A single VoIP or analog telephone interface
- A single USB conferencing endpoint
- Gating microphone automixing, with mix-minus matrix for voicelift
- As many as 16 overhead zones
- 2 sets of stereo codec/program outputs

Download the Q-SYS design files **Conf-System-110f w Expansion.qsys** and **Conf-System-Expansion 110f.qsys** at **http://www.qsc.com/resource-files/productresources/dn/dsp_cores/core_110f/q_dn_core_110f_appguide_expansion_examples.zip**

System wiring

Using these configurations, the first eight conferencing microphones will connect to inputs 1 to 8 on the main core (see Figure 1). Microphones 9 to 24 will connect to inputs 1 to 8 and flex connections 1 to 8 on the expansion core (see Figure 2). Microphone mute buttons and LED control signals will wire to the corresponding GPIO input/outputs. The room outputs are wired to the outputs of both units, starting with output 1 of the main core. If used, the analog telephone line will connect to the main unit as will the USB. See the below diagrams for reference.

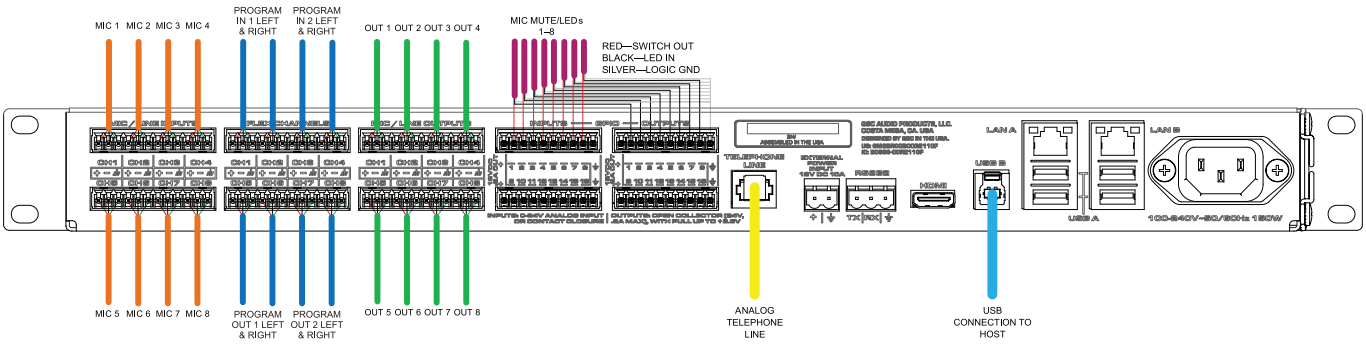


Figure 1. Wiring the main core processor

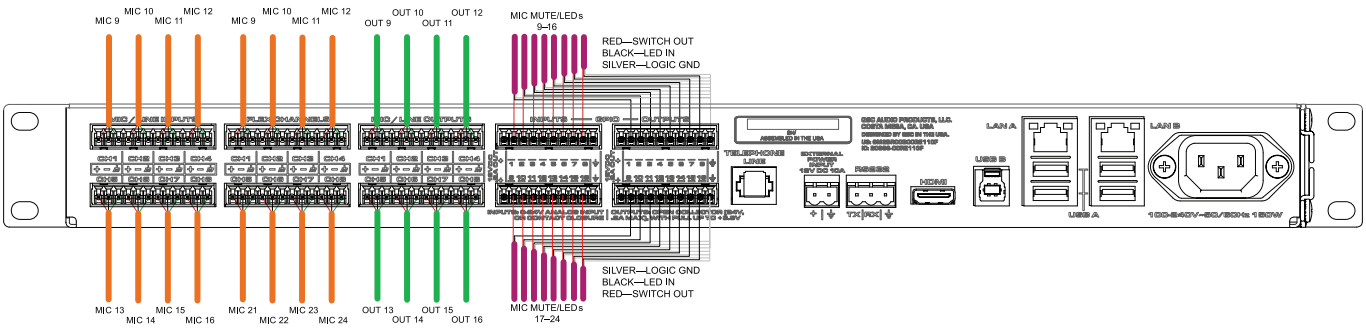


Figure 2. Wiring the expansion core processor

Deploying the configurations

Start the Q-SYS Designer software by opening the file **Conf-System-110f w Expansion.qsd**. This is the configuration for the main unit. Under **Tools**, open **Q-SYS Configurator**.

Discover each core processor in Q-SYS Configurator and set distinct IP addresses for them on the correct IP network. Give the main unit the name **MainCore** (Figure 3). Name the expansion unit **AECExpansion**. Note that if multiple systems like these are to be deployed on the same network, the names of each Q-SYS Core Processor and peripheral must be distinct. See the section on multiple deployments for that procedure.

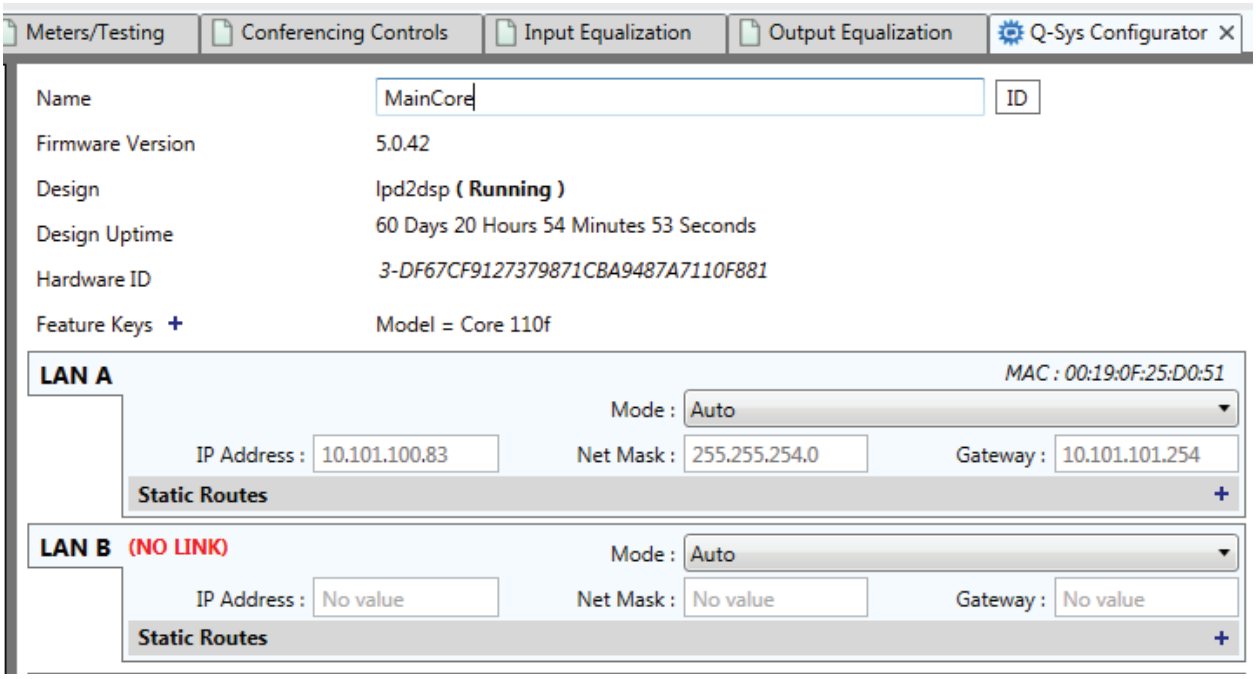


Figure 3. Naming the core processor in Q-SYS Configurator.

With the main core processor now properly named, save the Q-SYS design file to it by pressing **F5** or selecting **File > Save to Core & Run**.

Next, open the expansion core processor's design file, **Conf-System-Expansion 110f.qsd**. Now save that configuration to the core **AECExpansion** the same way, by pressing **F5** or selecting **File > Save to Core & Run**. Disconnect the expansion core processor by pressing **F7** or selecting **File > Disconnect**. All operations hereafter will be conducted connected only to the main core processor.

Deploying multiple systems on the same network

As mentioned before, if multiple systems are to be deployed on the same network, the systems must all have distinctive names. For example, if a Q-SYS network spans two rooms, conference rooms 101 and 102, and each has its own system, the main core processors might be named **MainCore101** and **MainCore102**, and the respective expansion processors **ExpansionCore101** and **ExpansionCore102**. Use Q-SYS Configurator to rename these devices.

To save the main design file we've been working with to the core **MainCore101**, the MainCore unit needs to be renamed in the design. (You will do the same later with **MainCore102**.)

First, select the **Core : MainCore** processor in the design inventory (Figure 4).

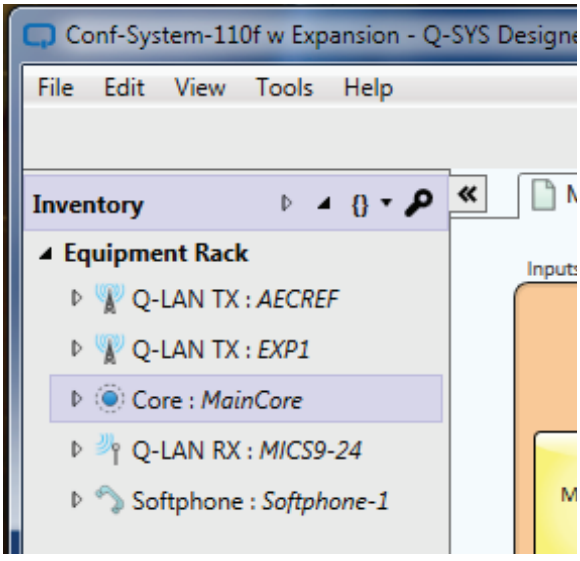


Figure 4. Select MainCore in the design inventory.

In the **Core Properties** panel, change its name to **MainCore101** (Figure 5). This will ensure that the design reaches the correct core processor.

Now that the name of the main core in the design matches the name of the actual device, you can save the design into the core processor. Press **F5** or select **File > Save to Core & Run**. Repeat this process for **MainCore102**.

Open the design file for the expansion core processors. Rename the core processor to **ExpansionCore101** and press **F5** or select **File > Save to Core & Run** to save it to the core processor with that name. Next, rename the core processor in the design to **ExpansionCore102** and then save the design to that core processor.

Press **F7** or select **File > Disconnect** to disconnect from the expansion core processor.

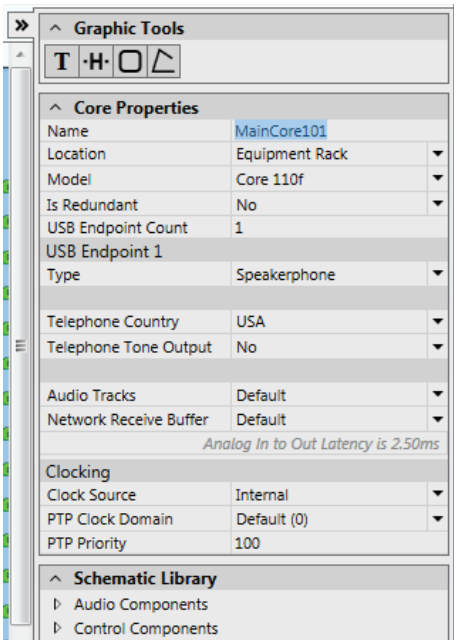


Figure 5. Rename MainCore to MainCore101.

Configuring telephony and USB

VoIP telephony and USB will require configuration before you can make conference calls. To configure VoIP, please see the appropriate QSC document for configuring Q-SYS with a compatible phone system. These documents are available on the QSC web site at **http://www.qsc.com/resources/document-library/**.

To configure a conferencing application such as Skype for Business™ to use the Core 110f for conferencing, plug the host computer (PC, Mac, or Chrome OS) into the main core processor's USB B port. The computer's USB port should detect the core processor automatically and install the drivers.

The design file for the main core processor that will handle conference calls specifies one USB endpoint in the **Core Properties** panel, designated as a **Speakerphone**.

System setup

The main core design file includes a User Control Interface (UCI) that provides the controls needed for operating both Core 110f processors as one conferencing system.

Open **Q-SYS UCI Viewer**. Locate the design for MainCore101 and open the System Setup UCI associated with it. The UCI has multiple pages of setup guidance. Follow the steps to set up the system.

Please note that the UCI does not include EQ settings. Instead, there are pages in the design schematic for input (Figure 6) and output (Figure 7) EQ.

Figure 6. Input (microphone) EQ.

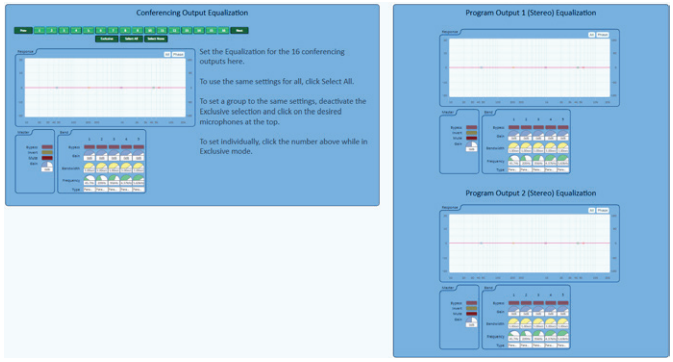


Figure 7. Output EQ.

External control considerations

The design for the main core processor includes an extensive list of named controls for use with an AMX, Crestron, or other third-party controller.

Microphone mutes: **micmute1** through **micmute24**

Program inputs: **pgmlevel1**, **pgmlevel2**, **pgmmute1**, **pgmmute2**

Analog telephony: **potsrxlevel**, **potsrxmute**, **potstxlevel**, **potstxmute**

VoIP telephony: **voiprxlevel**, **voiprxmute**, **voiptxlevel**, **voiptxmute**

USB: **usbrxlevel**, **usbrxmute**, **usbtxlevel**, **usbtxmute**

Below are the named controls for analog and VoIP telephony control.

- Keypad: **voip1**, **voip2**, **voip3**, **voip4**, **voip5**, **voip6**, **voip7**, **voip8**, **voip9**, **voip0**, **voip***, **voip#**, **pots1**, **pots2**, **pots3**, **pots4**, **pots5**, **pots6**, **pots7**, **pots8**, **pots9**, **pots0**, **pots***, **pots#**
- Dial string: **voipdialstring**, **voipbacksp**, **voipclr**, **potsdialstring**, **potsbacksp**, **potsclr**
- Call control: **voipconnect**, **voipdisconnect**, **voipflash**, **voipdnd**, **potsconnect**, potsdisconnect, **potsflash**, **potsdnd**
- Call status feedback strings: **voipcallstatus**, **potscallstatus**
- Contact lists: **potslists**, **potsnames**, **potssearch**, **potsnumber**, **voiplists**, **voipnames**, **voipsearch**, **voipnumber** (Contact lists are configured in Q-SYS Administrator.)

For details on using named controls in this context, please see the Q-SYS help file.

Understanding the DSP signal flow

See Figure 8. A single Core 110f processor provides as many as 16 AEC processing channels. Each channel's processing takes place in the DSP of the same processor that its conference mic is attached to. Therefore, the AEC processing in the expansion core processors requires a reference signal, just as in the main core. The reference signal is delivered to the expansion processors via Q-LAN; the links are already in place in the designs. Similarly, control links are in place so that microphone gain controls, mute controls, and AEC features such as bypass and noise reduction in the expansion core processor are controlled through the main core processor.

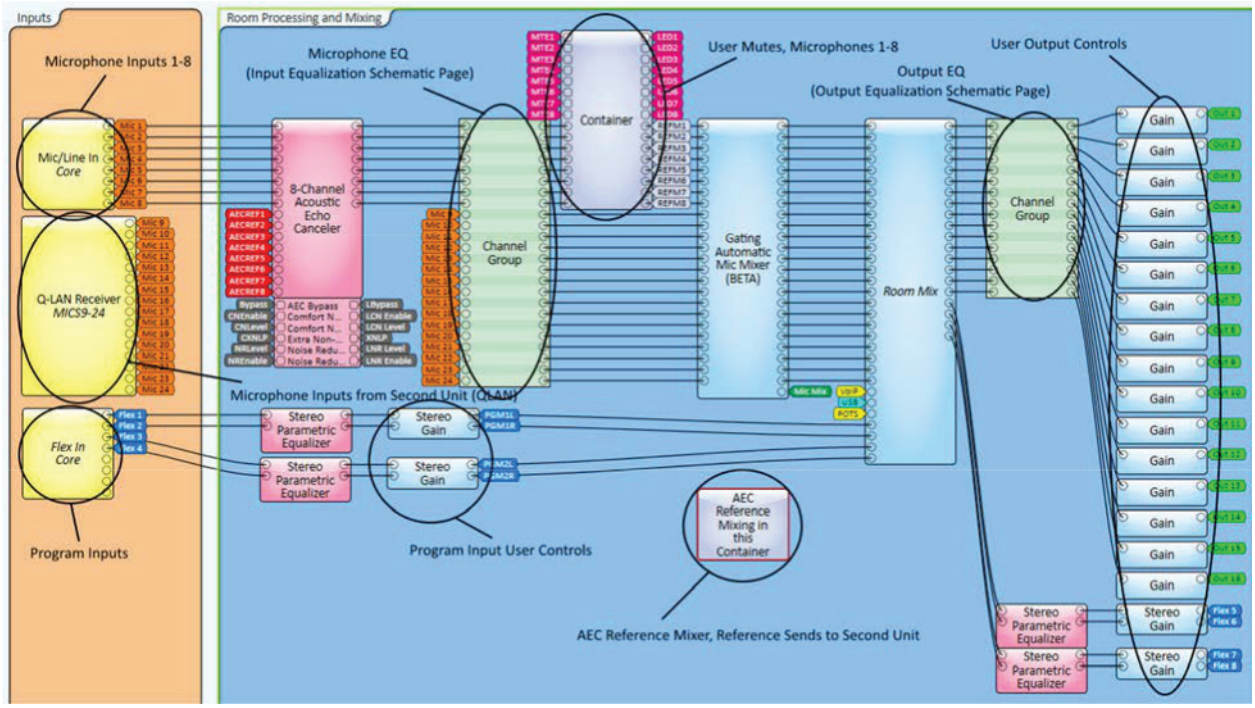


Figure 8. Conference mic inputs and their processing in the main core processor.

These designs do not use the local reinforcement output of the AEC, so comfort noise in the AEC block must be turned off so it is not heard in the room. Instead, the gating automixer is set for “last mic hold,” so the far end party to the phone call will hear some noise from the room. This will sound more natural than comfort noise.

The channel group in the main core processor’s design contains the high-pass filtering and parametric EQ for all the conference mics, including the ones connected to the expansion core processor. Other schematic pages contain input and output EQ, making it simple to make necessary adjustments.

For simplicity, all mixing is done in the main core processor. A matrix mixer for the room follows the gating automatic mic mixer; the room mix is set up in the System Setup UCI, as is the composition of the AEC references.

The main core processor receives all the far end sources—POTS, VoIP, or USB—with a separate gain control on each input (Figure 9). At the transmit end, an 8×3 matrix mixer provides a separate mix for each of the three signals available to send to far ends.

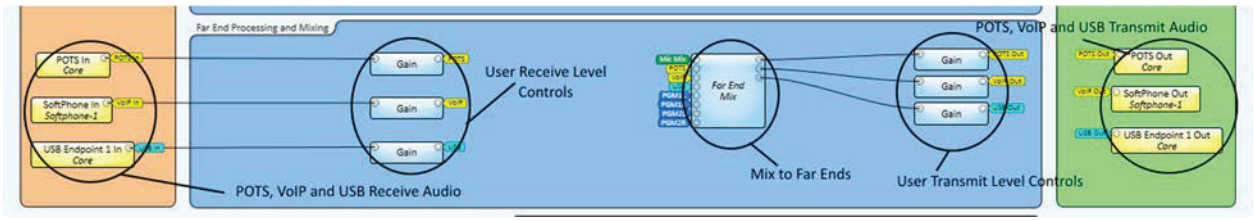


Figure 9. Handling inputs from, and outputs to, the far end(s).

Room outputs 1 through 8 go to the line outputs of the main core processor, while 9 through 16 go via Q-LAN to the expansion core processor (Figure 10). All 16 room outputs pass through the Mix-Minus AutoSetup block, which eliminates the slight echoes that result from a local signal passing through two paths with different propagation times.

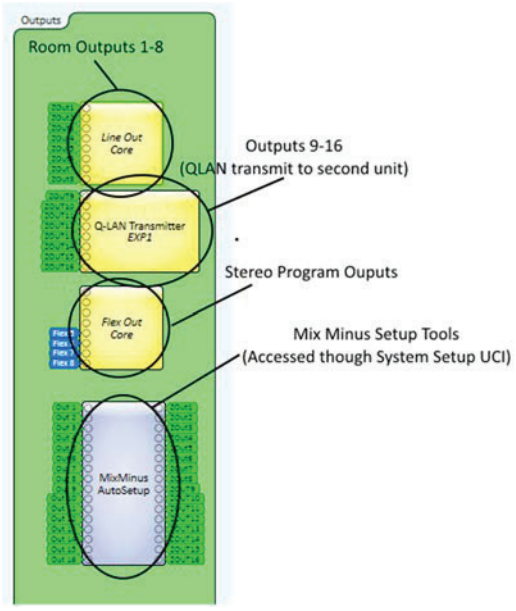


Figure 10. The output circuits in the main core processor.

Accessing the System Setup UCI for installation

The System Setup UCI will guide the installer through the process of setting up the signal flow.

In **Q-SYS UCI Viewer**, select the **System Setup UCI** (Figure 11).

To maximize the System Setup UCI on your desktop, click the **Hide Menu** and **Full Screen** icons (Figure 12).

Click **BEGIN** to proceed (Figure 13).

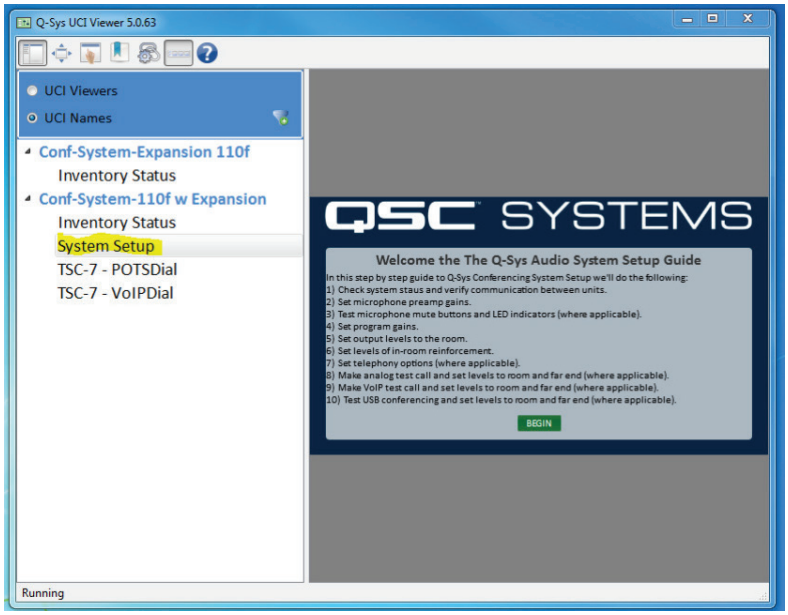


Figure 11. Select System Setup UCI in the Q-SYS UCI Viewer.

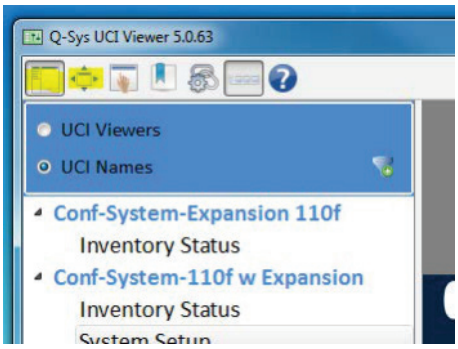


Figure 12. These options will maximize the UCI to fill your desktop.

Figure 13. The first screen of the System Setup UCI. Follow this procedure to set up the system.

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